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1. (Currently amended) A process for fabricating a complementary metal oxide semiconductor (CMOS) structure comprising:

providing a plurality of polySi gates overlying a semiconductor substrate, each polySi gate comprises a dielectric cap located on an upper surface thereof, wherein said dielectric cap comprises a first dielectric material;

forming silicided source/drain regions in the semiconductor substrate;

forming a ~~planarized~~ dielectric stack on the semiconductor substrate, wherein said dielectric stack comprises a first, lower dielectric layer and a second, upper dielectric layer, wherein the first, lower dielectric layer comprises the first dielectric material, and wherein the second, upper dielectric layer comprises a second, different dielectric material;

planarizing the dielectric stack to remove an upper portion of the second, upper dielectric layer;

performing an etching process to selectively remove the first, lower dielectric layer and the dielectric cap against the second, upper dielectric layer to thereby expose only an upper surface of each polySi gate, wherein the exposed upper surface of each polySi gate is below an upper surface of the second, upper dielectric layer; and

performing a salicide process which converts each polySi gate to a metal silicide gate, wherein each metal silicide gate has substantially the same height, is composed of the same silicide phase, and has substantially the same workfunction for the same polySi ion implant conditions.

2. (Original) The method of Claim 1 wherein the plurality of polySi gates are formed atop a gate dielectric.

3. (Original) The method of Claim 1 wherein the plurality of polySi gates are formed by deposition, lithography and etching.

4. (Original) The method of Claim 1 wherein the dielectric cap is composed of a nitride.

5. (Original) The method of Claim 1 wherein the step of providing the plurality of polySi gates includes the formation of at least one spacer on each exposed sidewall of the polySi gates.

6. (Original) The method of Claim 5 wherein the at least one spacer includes a first spacer and a second spacer, wherein the first spacer has a thickness that is narrower than the second spacer.

7. (Original) The method of Claim 1 wherein the step of forming the silicided contacts on source/drain regions comprises depositing a metal atop the semiconductor substrate, and performing a salicide process.

8. (Original) The method of Claim 7 wherein the metal comprises Ti, Ta, W, Co, Ni, Pt, Pd or alloys thereof.

9. (Original) The method of Claim 8 wherein the metal is Co, Ni or Pt.

10. (Original) The method of Claim 7 wherein the salicide process comprises a first anneal, a selective etching step and optionally a second anneal.

11. (Original) The method of Claim 7 further comprising forming a layer of silicon atop the semiconductor substrate prior to metal deposition.

12. (Currently amended) The method of Claim 1 wherein the ~~step of forming a planarized dielectric stack comprises deposition and planarization~~ first dielectric material is a nitride, and wherein the second, different dielectric material is an oxide.

13. (Currently amended) The method of Claim 1 wherein the step of ~~forming a planarized dielectric stack comprises forming an etch stop layer, forming an interlevel dielectric and planarizing the interlevel dielectric~~ comprises chemical mechanical polishing.

14. (Original) The method of Claim 1 wherein the etching process comprises a reactive ion etch step.

15. (Original) The method of Claim 1 wherein the salicide process comprises depositing a blanket silicide metal layer atop the at least the exposed upper surface of each polySi gate, first annealing to cause total or partial consumption of the polySi gates, selective etching non-reacted silicide metal and optionally performing a second anneal.

16. (Original) The method of Claim 15 wherein the silicide metal comprises Ti, Ta, W, Co, Ni, Pt, Pd or alloys thereof.

17. (Original) The method of Claim 16 wherein the silicide metal is Co, Ni or Pt.

18. (Original) The method of Claim 15 the first anneal is performed at a temperature from about 350° to about 550°C.

19. (Original) The method of Claim 15 wherein the optional second anneal is performed at a temperature from about 600°C to about 800°C.